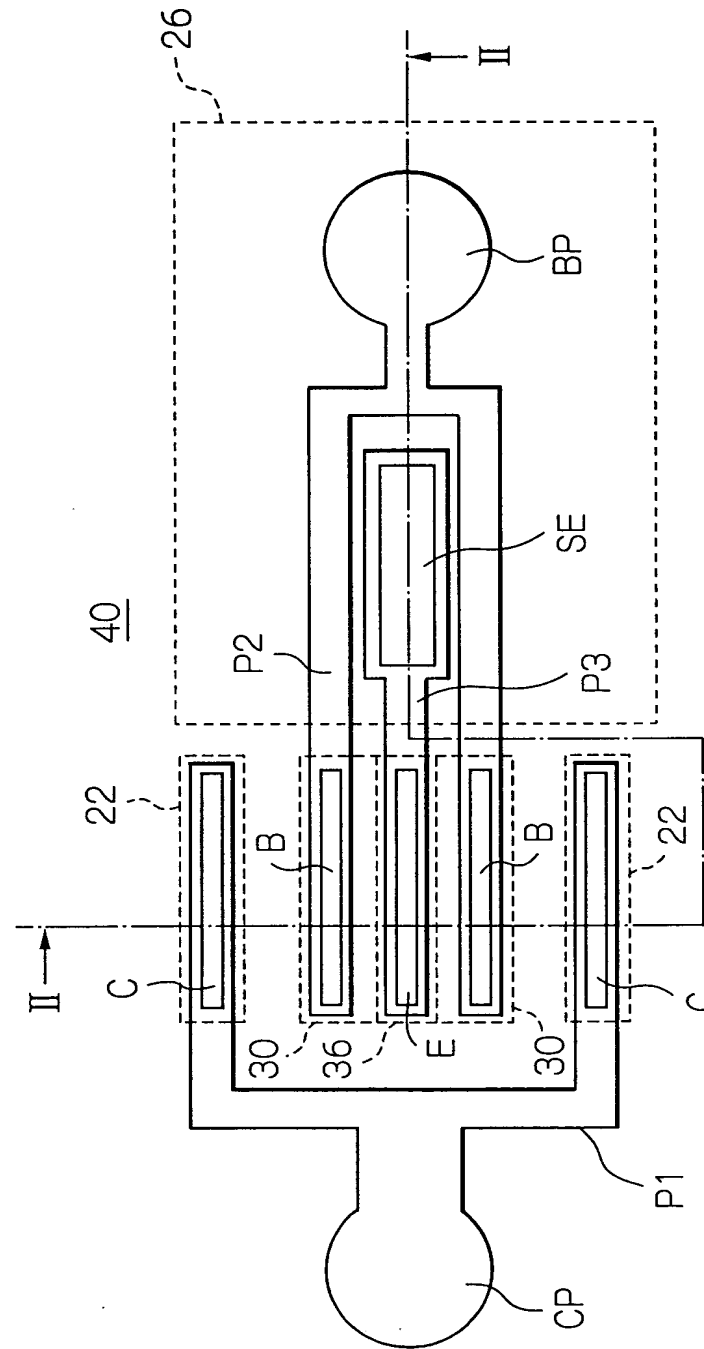
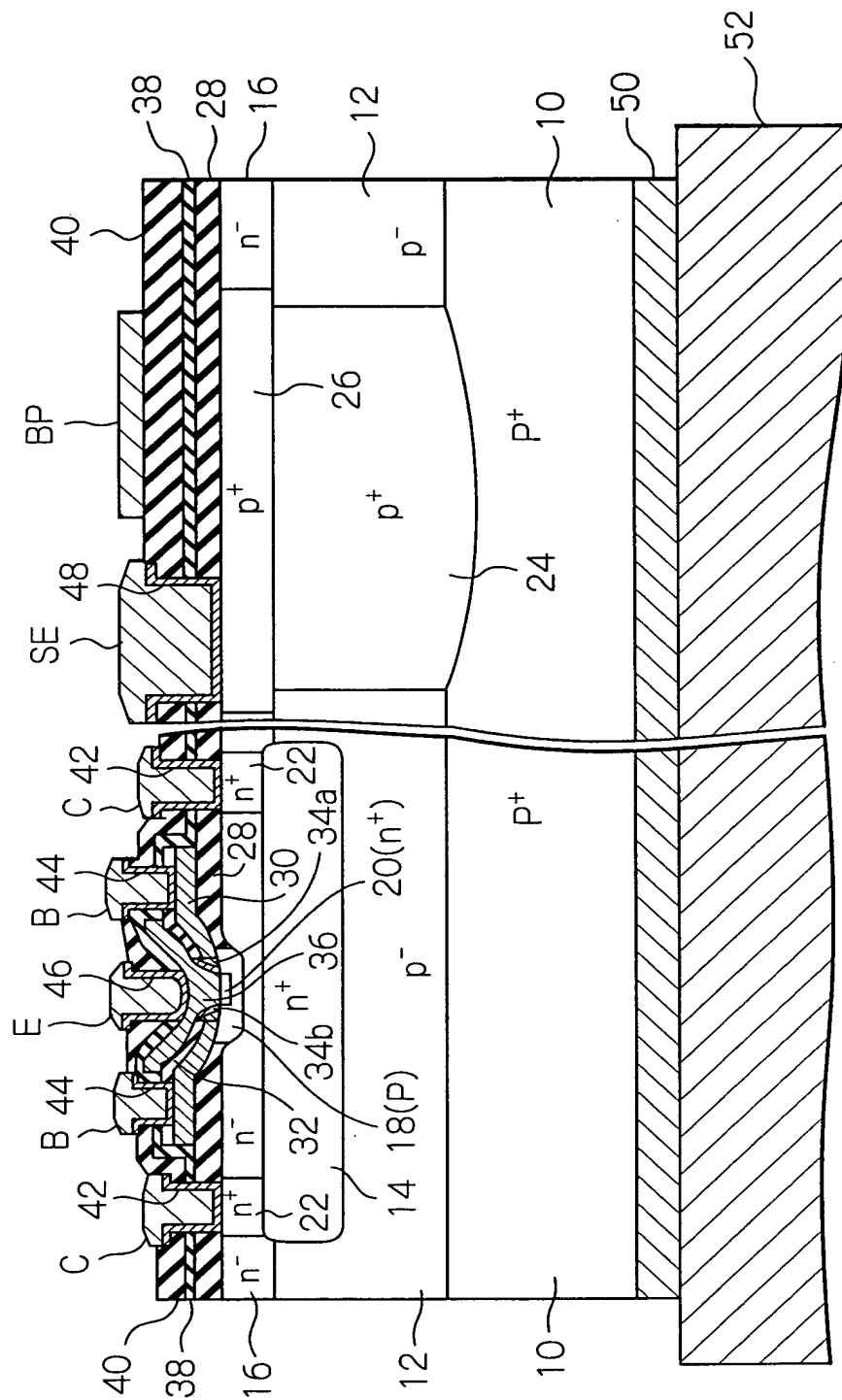


Fig. 1



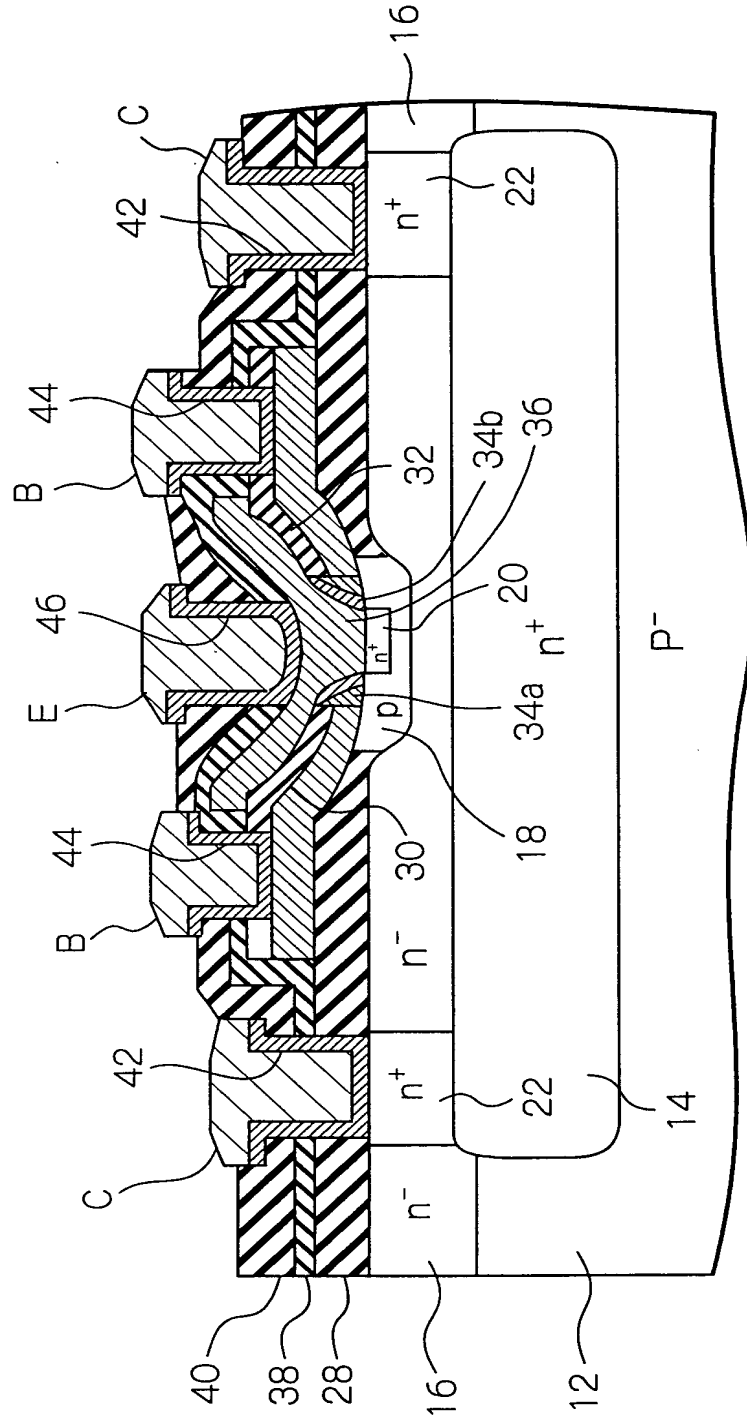
2/
25

Fig. 2



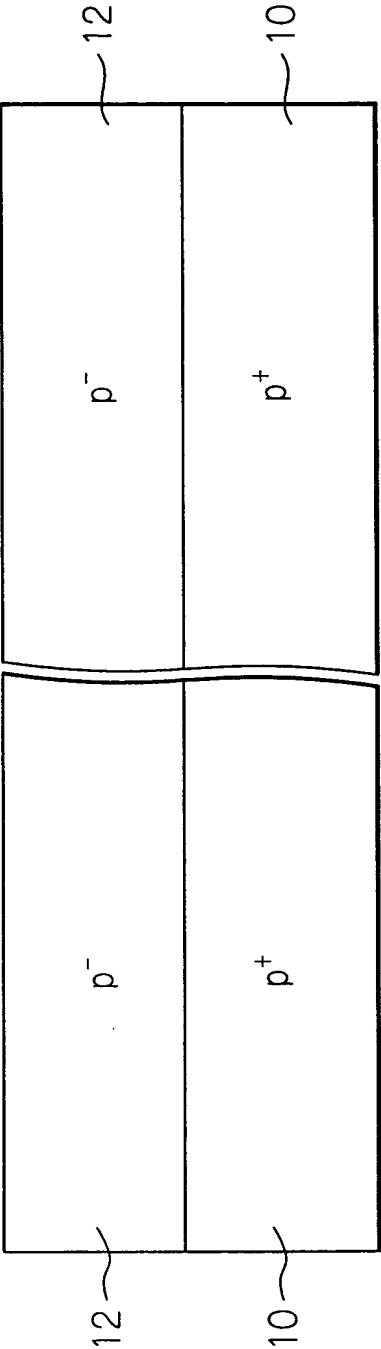
3
25

Fig. 3



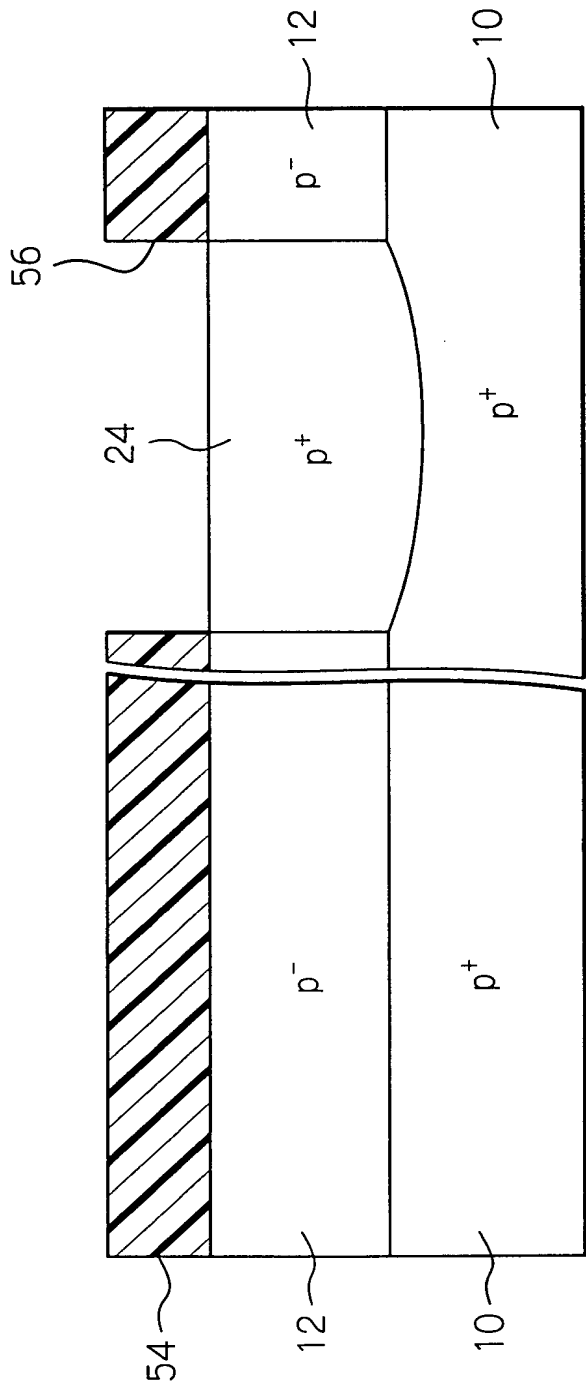
4/25

Fig. 4



5/25

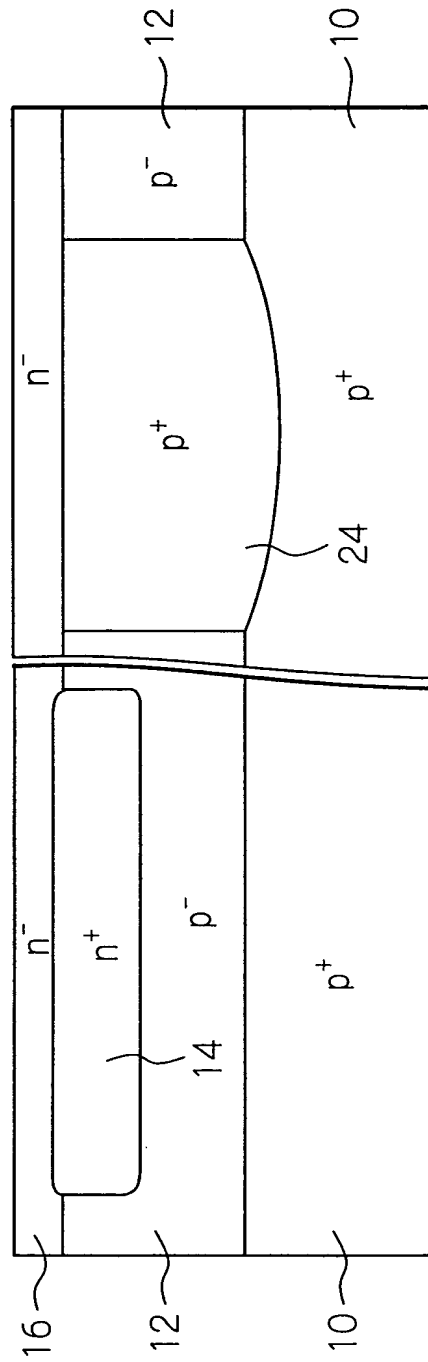
Fig. 5





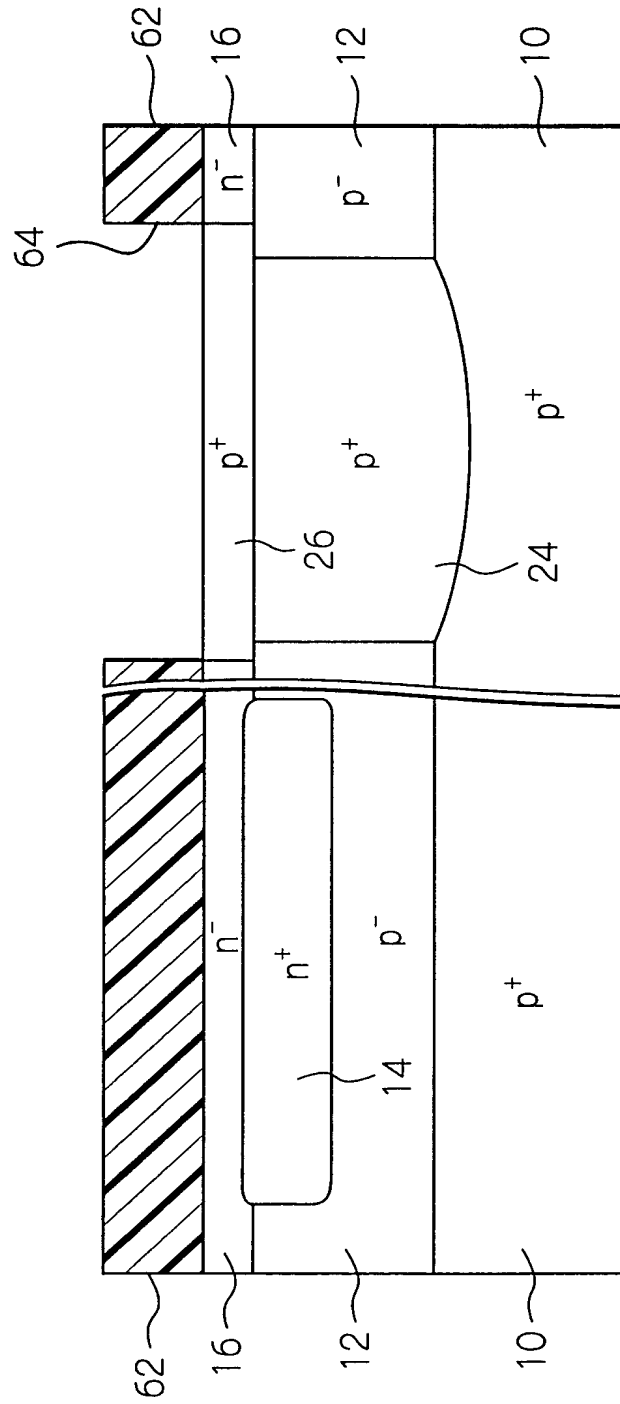
7/
25

Fig. 7



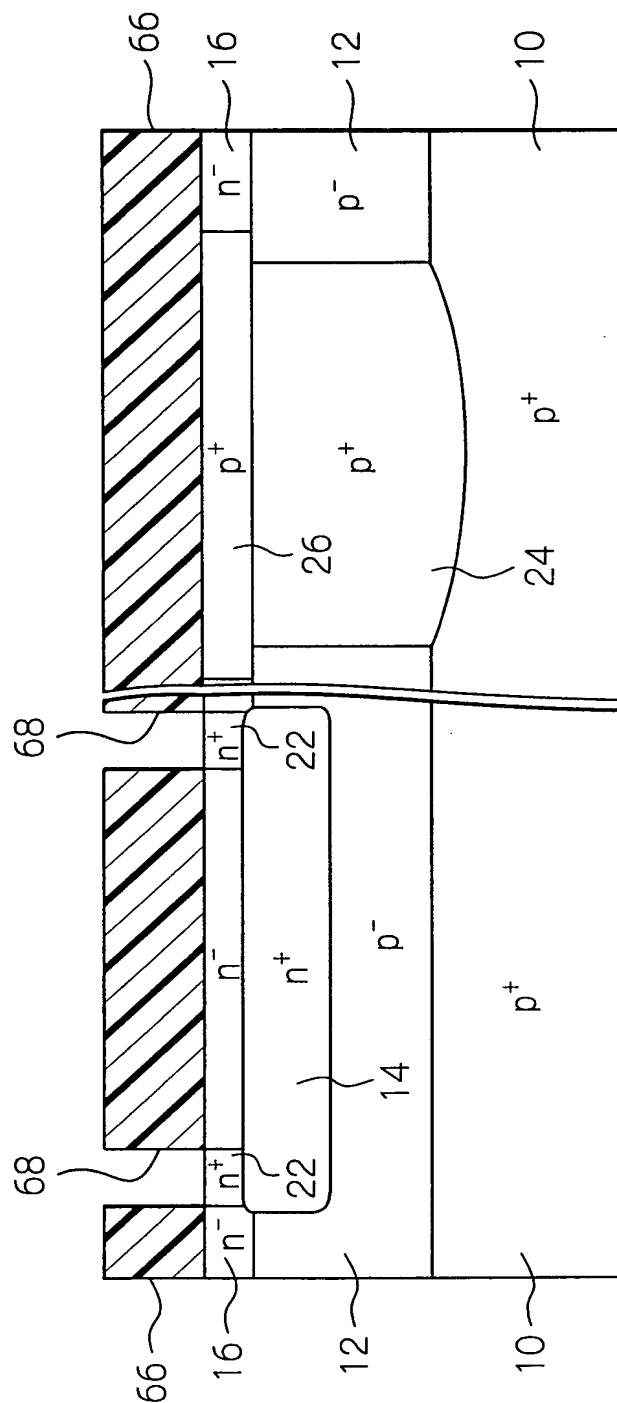
8/25

Fig. 8



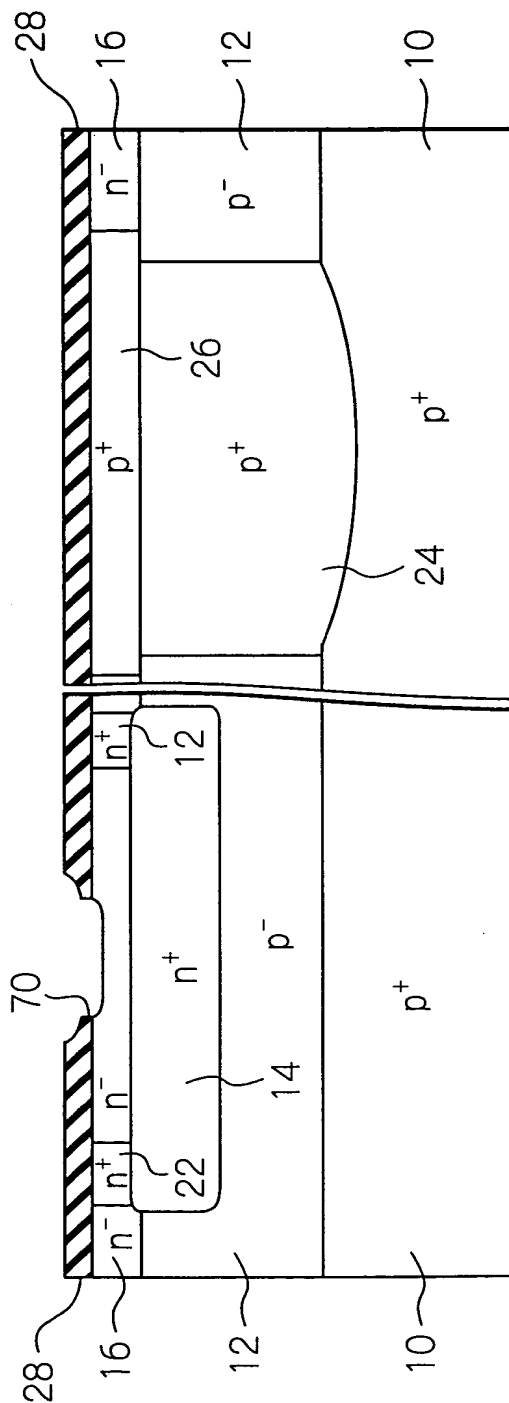
9/25

Fig. 9



10/25

Fig. 10



11/25

Fig. 11

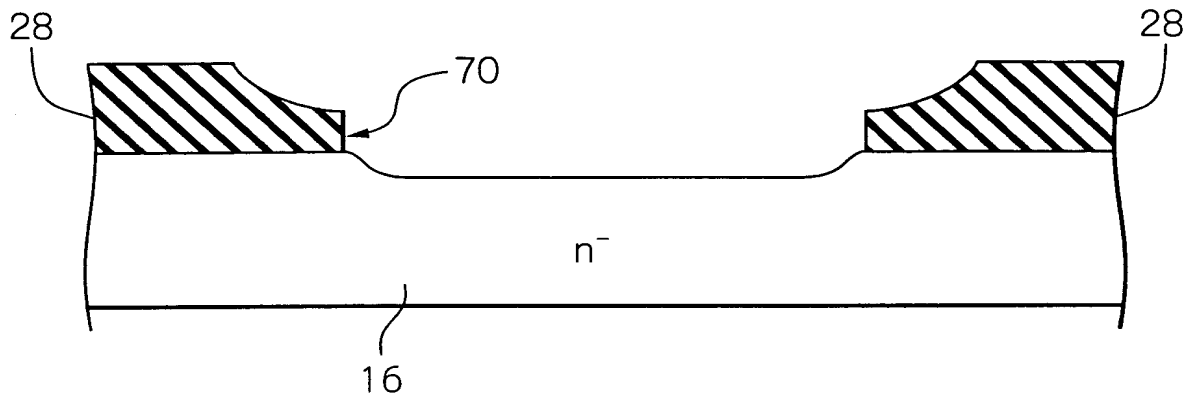
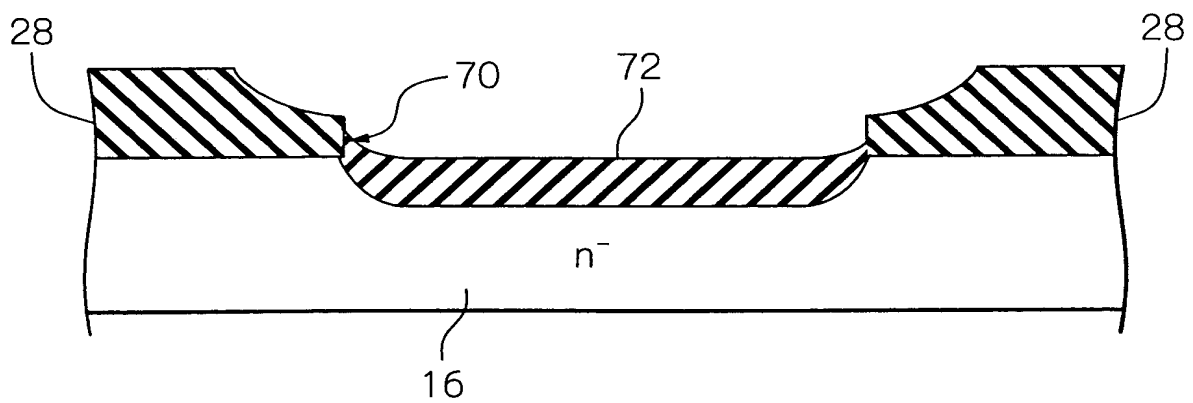
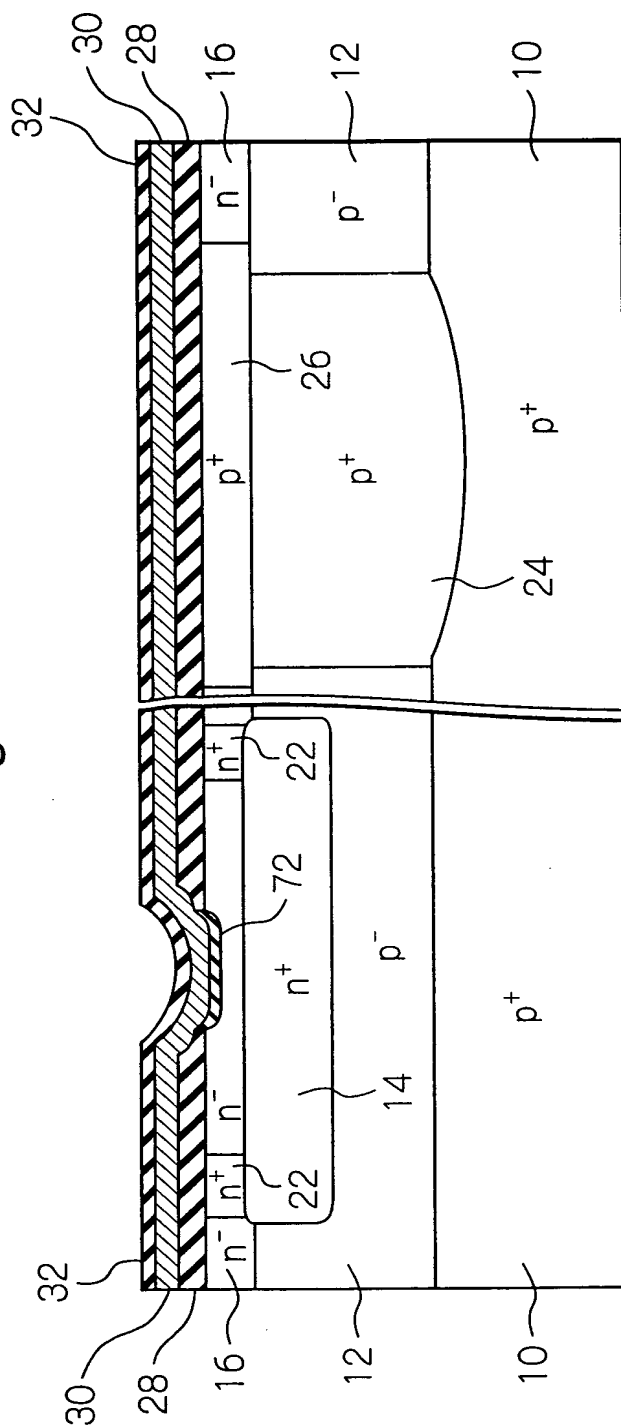


Fig. 12



12/25

Fig. 13



13/
25

Fig. 14

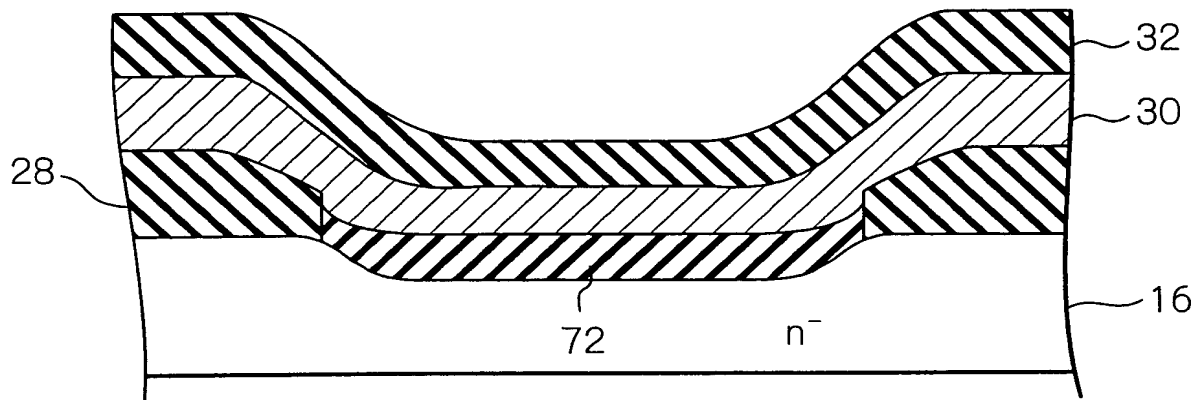
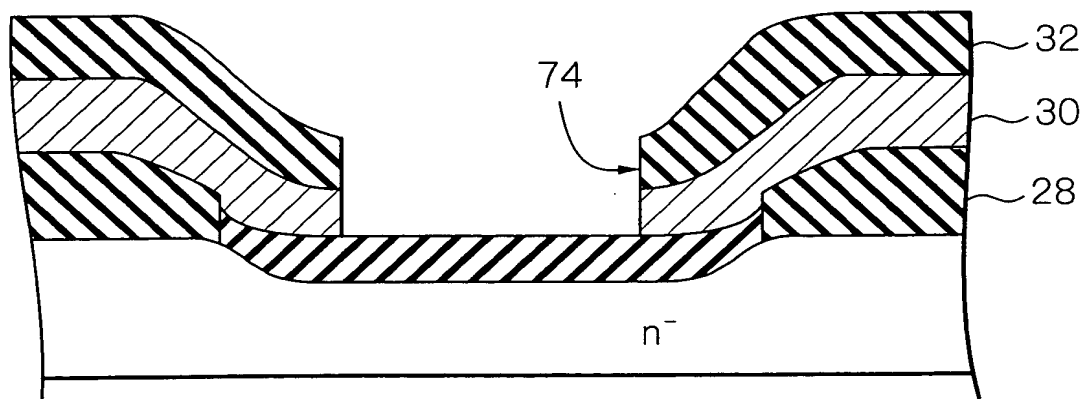


Fig. 15



14/
25

Fig. 16

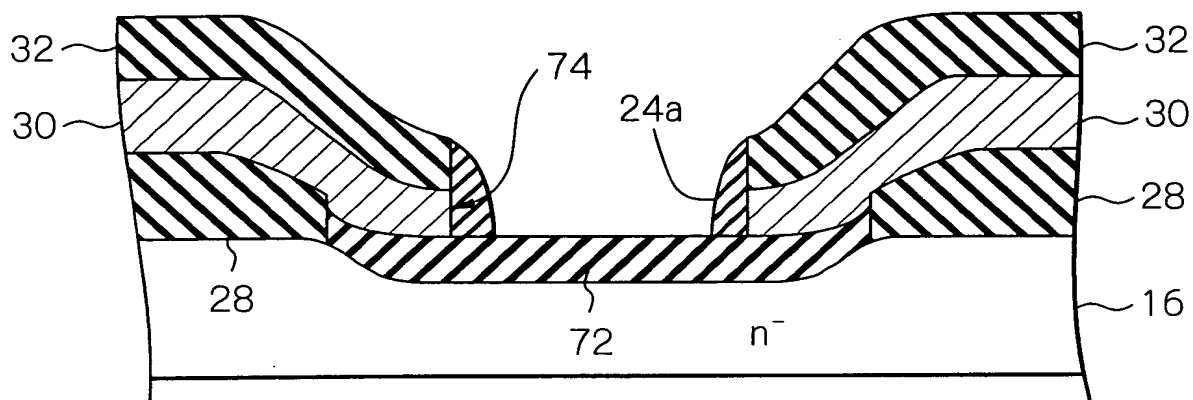
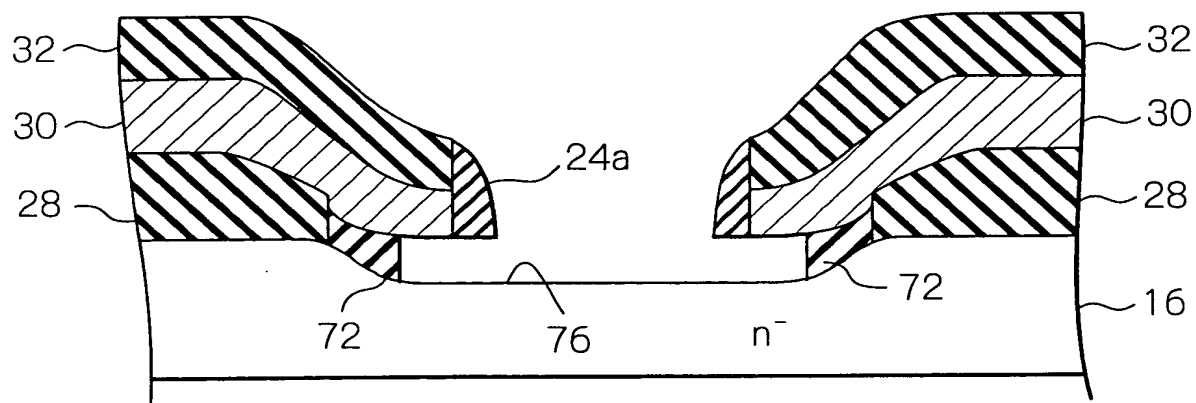


Fig. 17



15/
25

Fig. 18

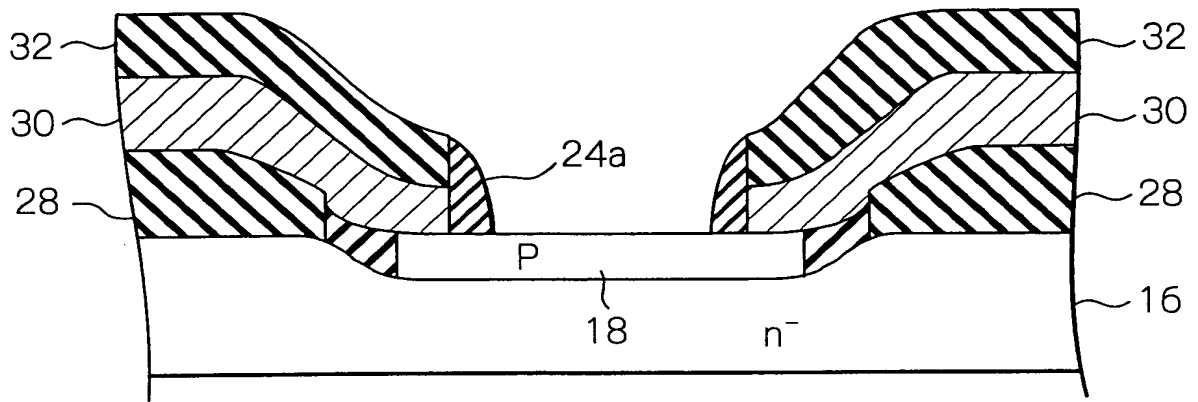
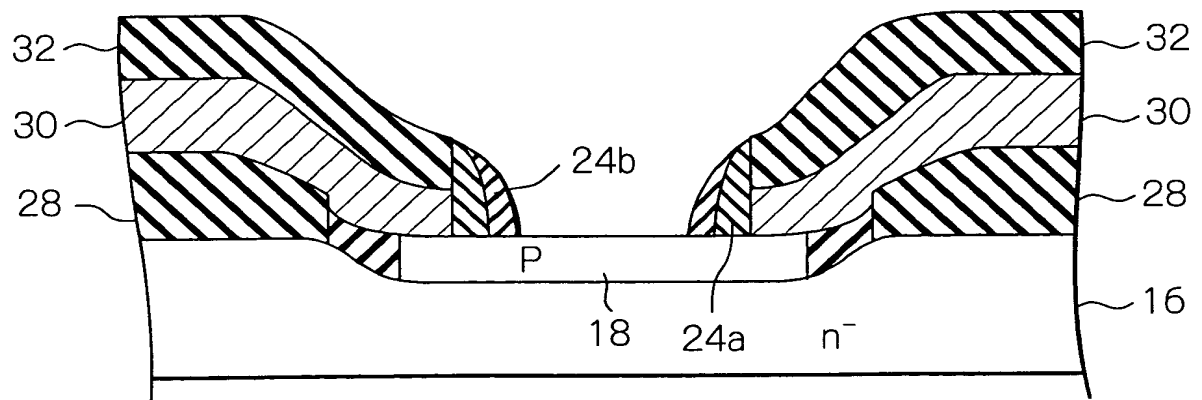


Fig. 19





17/
25

Fig. 21

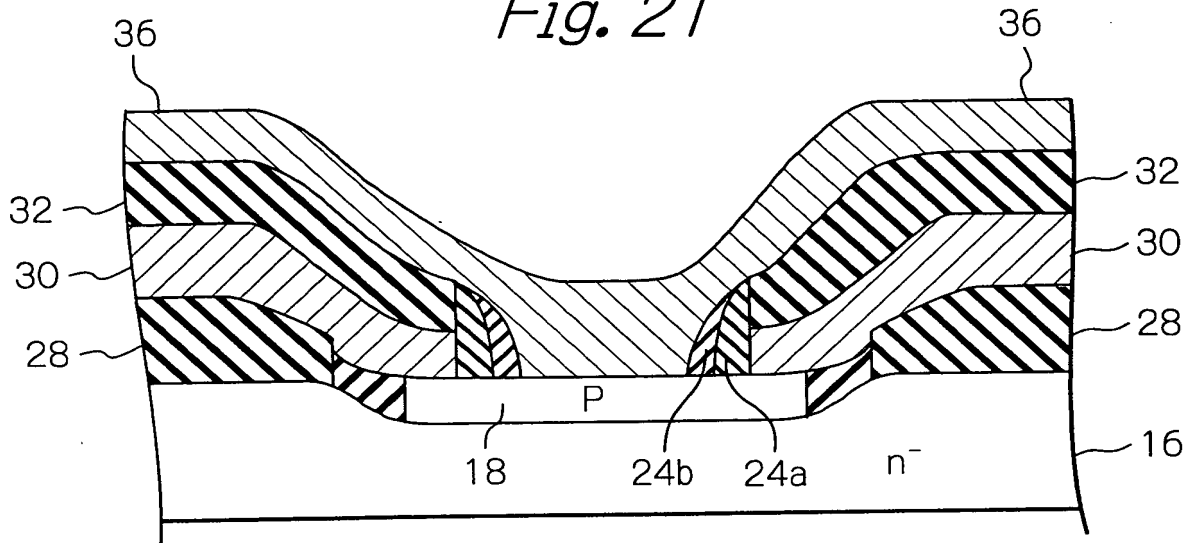


Fig. 22

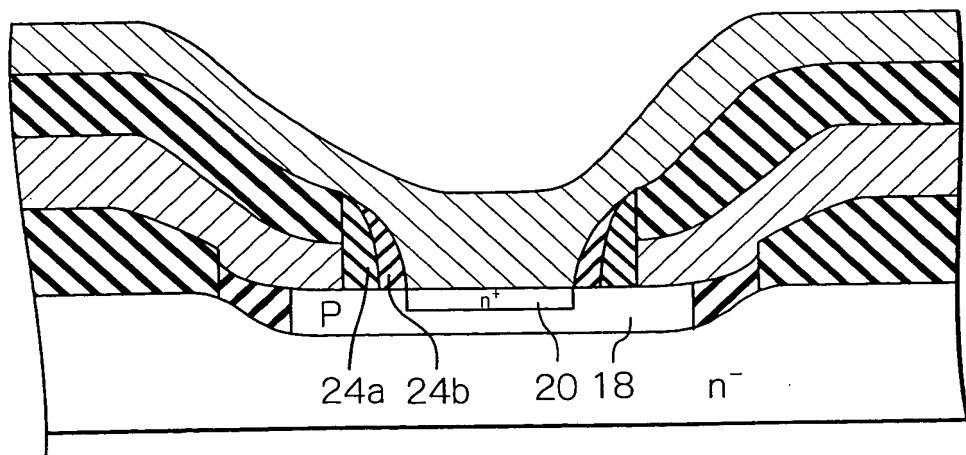
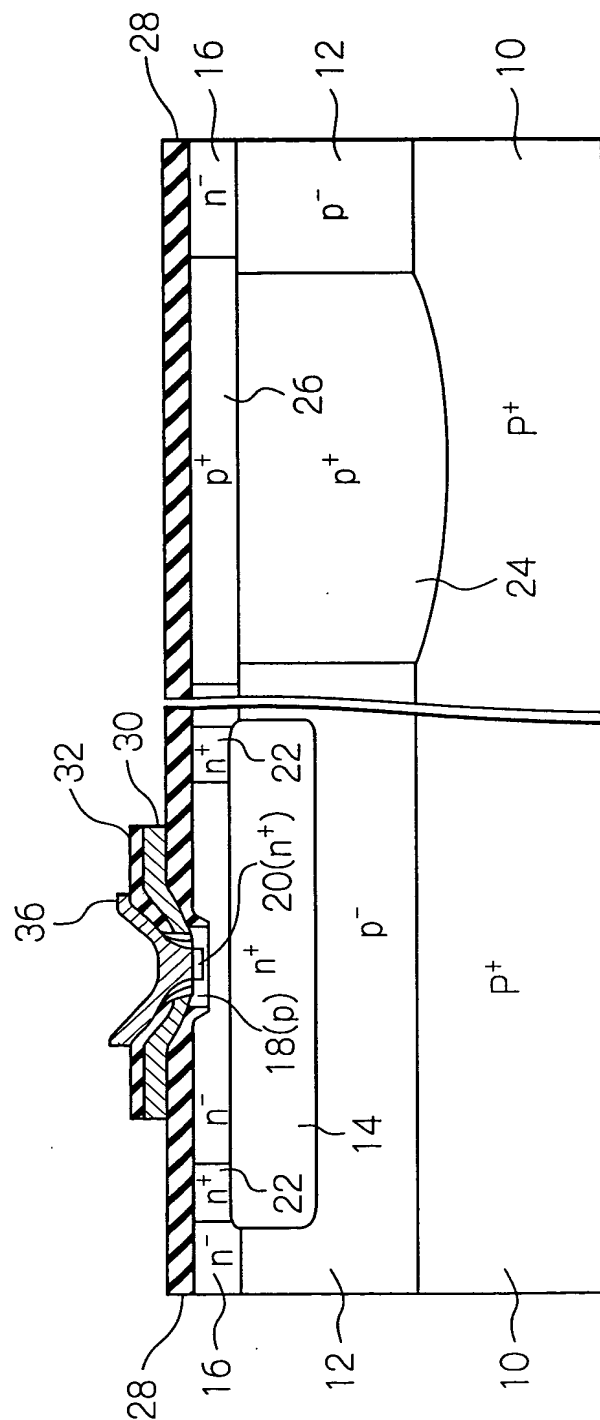
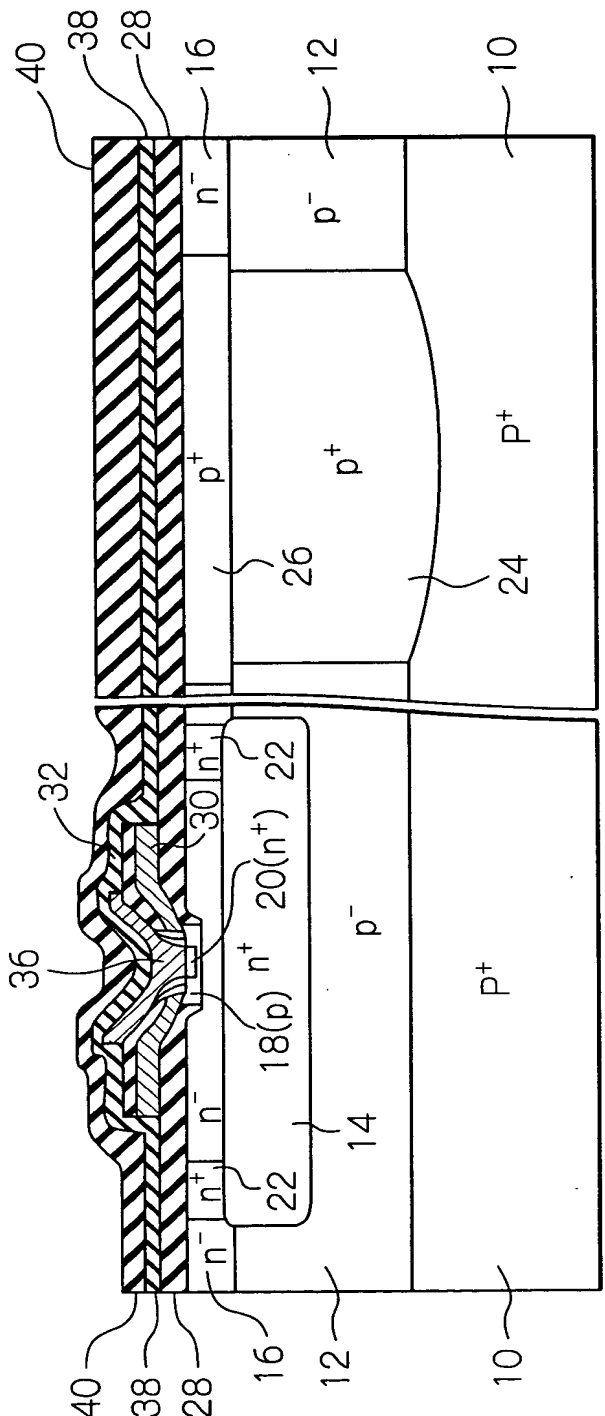


Fig. 23



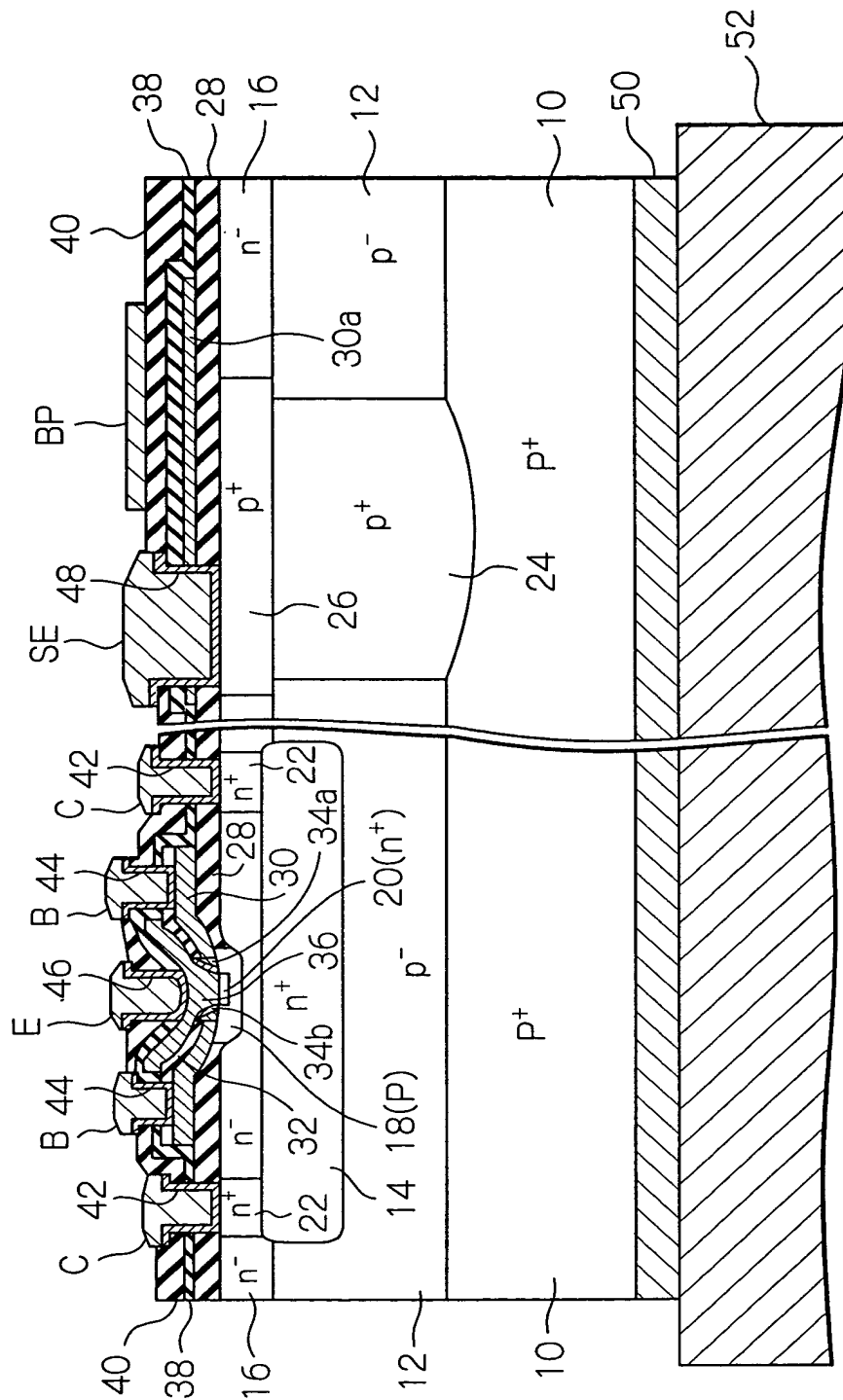
19/
25

Fig. 24



21/25

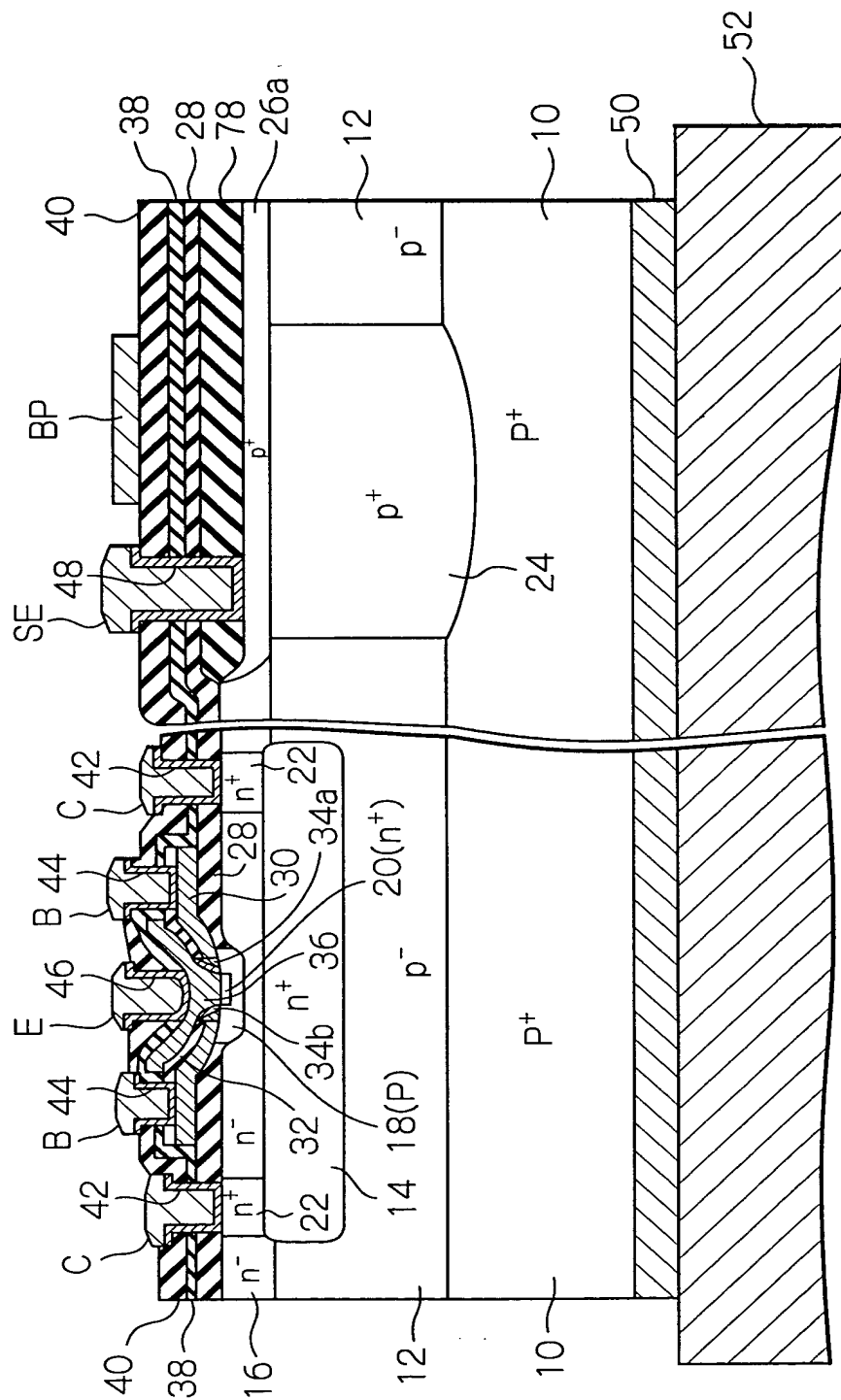
Fig. 26



This diagram shows a cross-section of a semiconductor device. The substrate consists of a p⁺ region (10) and an n⁻ region (12). A buried channel layer (14) is formed in the p⁺ region, containing n⁺ regions (16, 18(P), 20(n⁺)). A gate stack is formed on top of the substrate, including a gate oxide (22), a gate dielectric (24), and a gate electrode (26). The gate stack is divided into regions labeled 28, 30, 32, 34a, 34b, 36, 38, 40, 42, 44, 46, 48, and 50. A source/drain region (52) is formed in the n⁻ region. The device is shown in a cross-sectional view with various layers and regions labeled with numbers and symbols.

23/25

Fig. 28



$$\frac{24}{25}$$
